

# 74LVC2G240

Dual inverting buffer/line driver; 3-state

Rev. 04 — 29 February 2008

Product data sheet

## 1. General description

The 74LVC2G240 is a dual inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH level at pins  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G240 as a translator in a mixed 3.3 V and 5 V environment.

It is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

## 2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

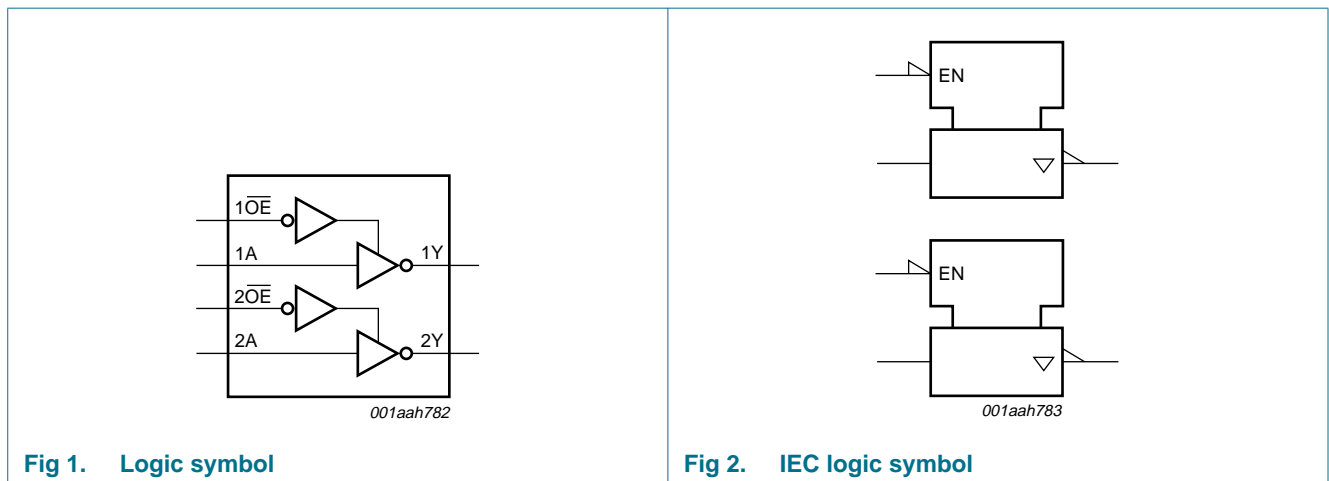
Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G240DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G240DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G240GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G240GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

### 4. Marking

Table 2. Marking codes

Type number	Marking code
74LVC2G240DP	V240
74LVC2G240DC	V40
74LVC2G240GT	V40
74LVC2G240GM	V40

### 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning

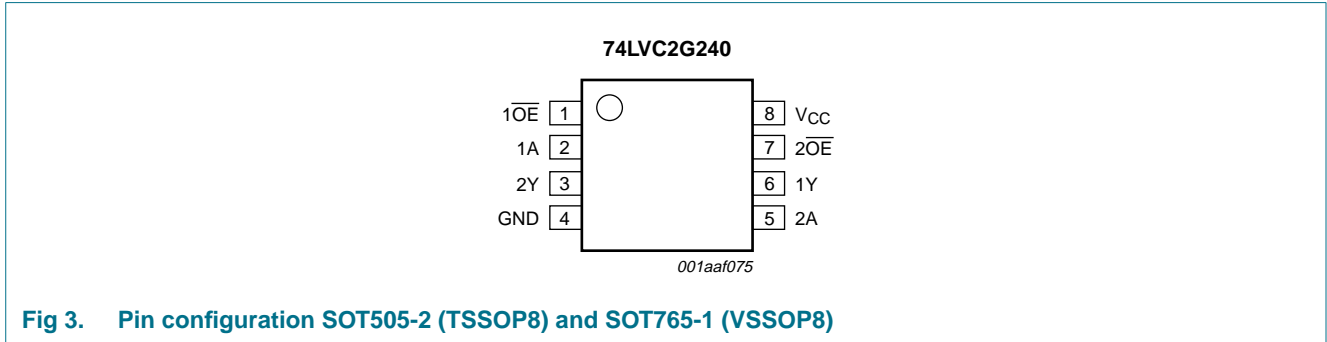


Fig 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

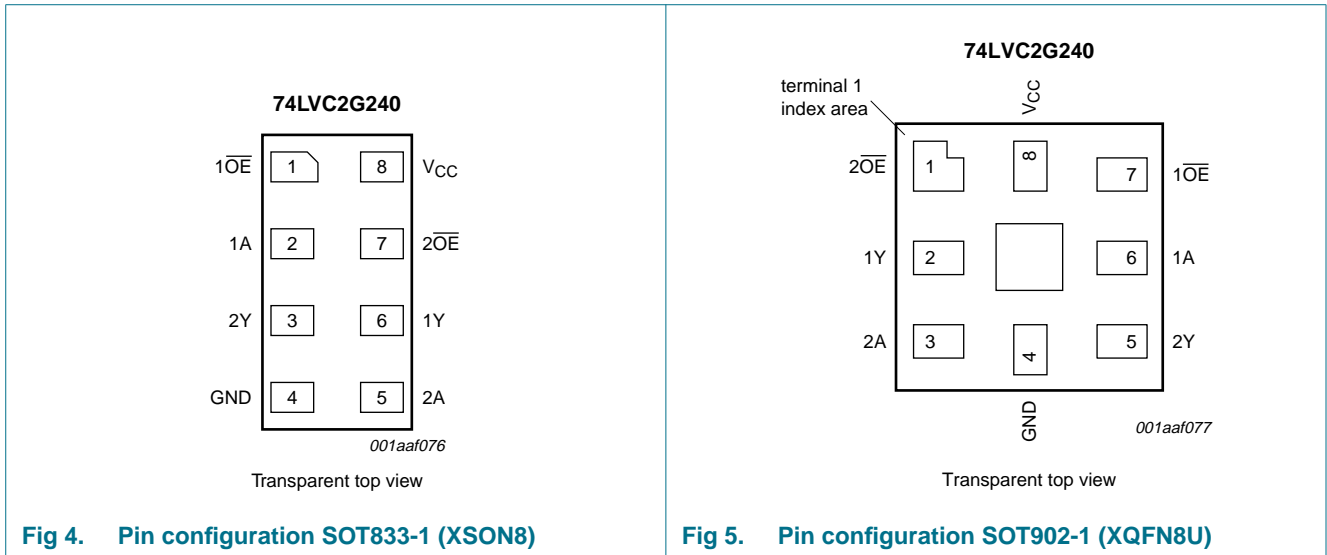


Fig 4. Pin configuration SOT833-1 (XSON8)

Fig 5. Pin configuration SOT902-1 (XQFN8U)

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1	SOT902-1	
1OE	1	7	output enable input 1OE (active LOW)
1A	2	6	data input
2Y	3	5	data output
GND	4	4	ground (0 V)
2A	5	3	data input
1Y	6	2	data output
2OE	7	1	output enable input 2OE (active LOW)
VCC	8	8	supply voltage

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Input		Output
nOE	nA	nY
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Enable mode	[1] -0.5	$V_{CC} + 0.5$	V
		Disable mode	[1] -0.5	+6.5	V
		Power-down mode	[1][2] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C the value of  $P_{tot}$  derates linearly at 2.5 mW/K.  
 For VSSOP8 packages: above 110 °C the value of  $P_{tot}$  derates linearly at 8.0 mW/K.  
 For XSON8 and XQFN8U packages: above 45 °C the value of  $P_{tot}$  derates linearly at 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V};$ Enable mode	0	$V_{CC}$	V
		$V_{CC} = 1.65\text{ V to }5.5\text{ V};$ Disable mode	0	5.5	V
		$V_{CC} = 0\text{ V};$ Power-down mode	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	-	-	V
$I_I$	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-	$\pm 0.1$	$\pm 5$	$\mu\text{A}$

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit		
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	±0.1	±10	µA		
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	±0.1	±10	µA		
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 1.65 V to 5.5 V	-	0.1	10	µA		
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 5.5 V	-	5	500	µA		
C <sub>I</sub>	input capacitance		-	2	-	pF		
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>								
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V		
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V		
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V		
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V		
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V		
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V		
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V		
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V		
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V		
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V		
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V		
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V		
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V		
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±20	µA		
		I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	-	±20	µA
		I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	-	±20	µA
		I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	40	µA
		ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 5.5 V	-	-	5	mA

[1] Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.1	9.5	1.0	11.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.6	5.2	0.5	6.5	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.0	5.5	1.0	6.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.5	4.6	0.5	5.8	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	2.0	4.0	0.5	5.0	ns
t <sub>en</sub>	enable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[3]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	4.5	10.3	1.5	12.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.9	5.6	1.0	7.0	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	5.6	1.5	7.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.5	4.7	0.5	5.9	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	2.0	3.8	0.5	4.8	ns
t <sub>dis</sub>	disable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.5	11.6	1.0	14.1	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.9	5.8	0.5	7.6	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	4.5	1.0	5.8	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	4.4	1.0	5.7	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.9	3.4	0.5	4.6	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>						
		output enabled	-	18	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>

[3] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>

[4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

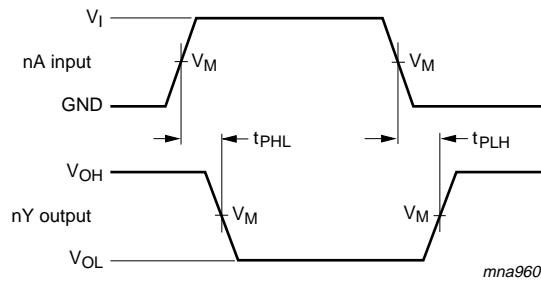
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

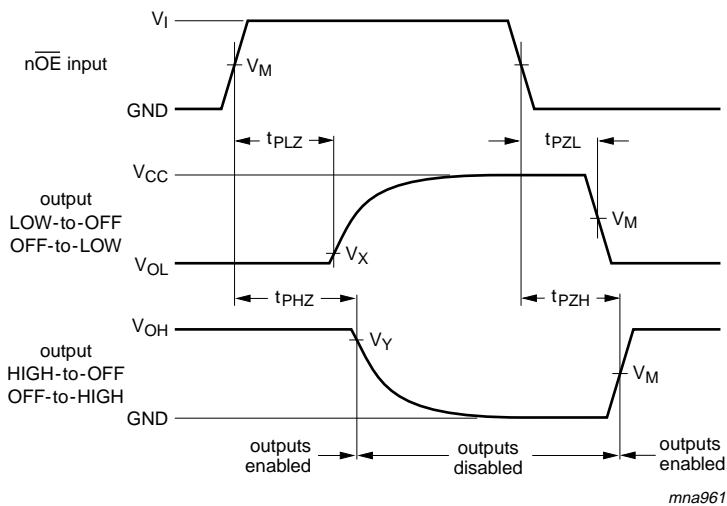
12. Waveforms



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The data input (nA) to output (nY) propagation delays**



Measurement points are given in [Table 9](#).

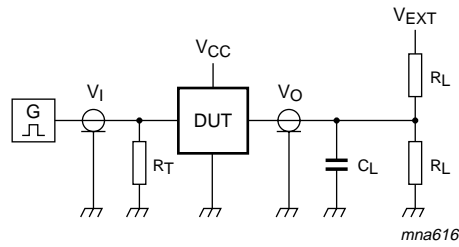
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. 3-state enable and disable times**

**Table 9. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$





Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Load circuitry for switching times**

**Table 10. Test data**

Supply voltage	Input	Load		$V_{EXT}$		
	$V_I$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	30 pF	1 k $\Omega$	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	30 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 $\Omega$	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 $\Omega$	open	GND	6 V
4.5 V to 5.5 V	$V_{CC}$	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

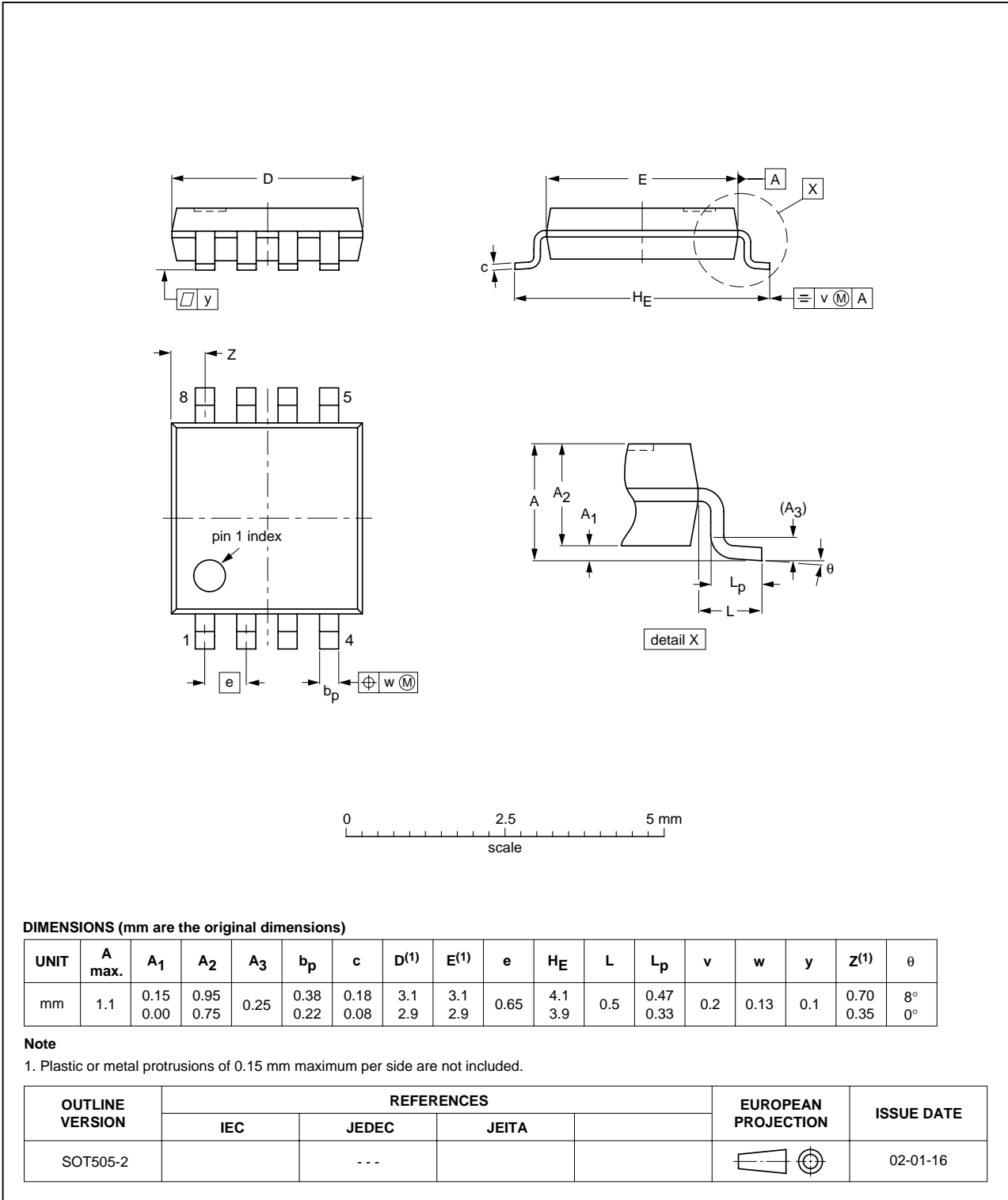


Fig 9. Package outline SOT502-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

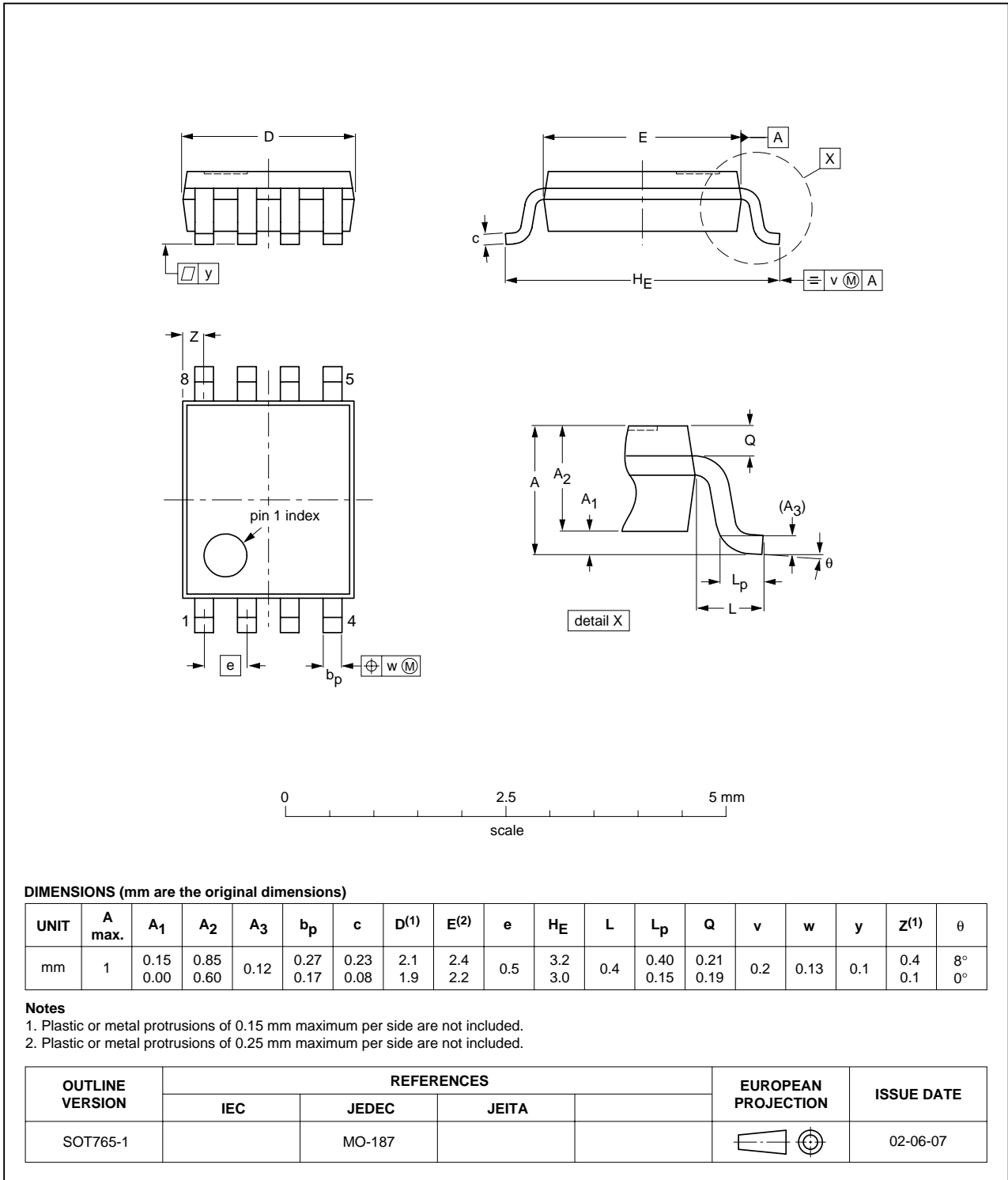


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

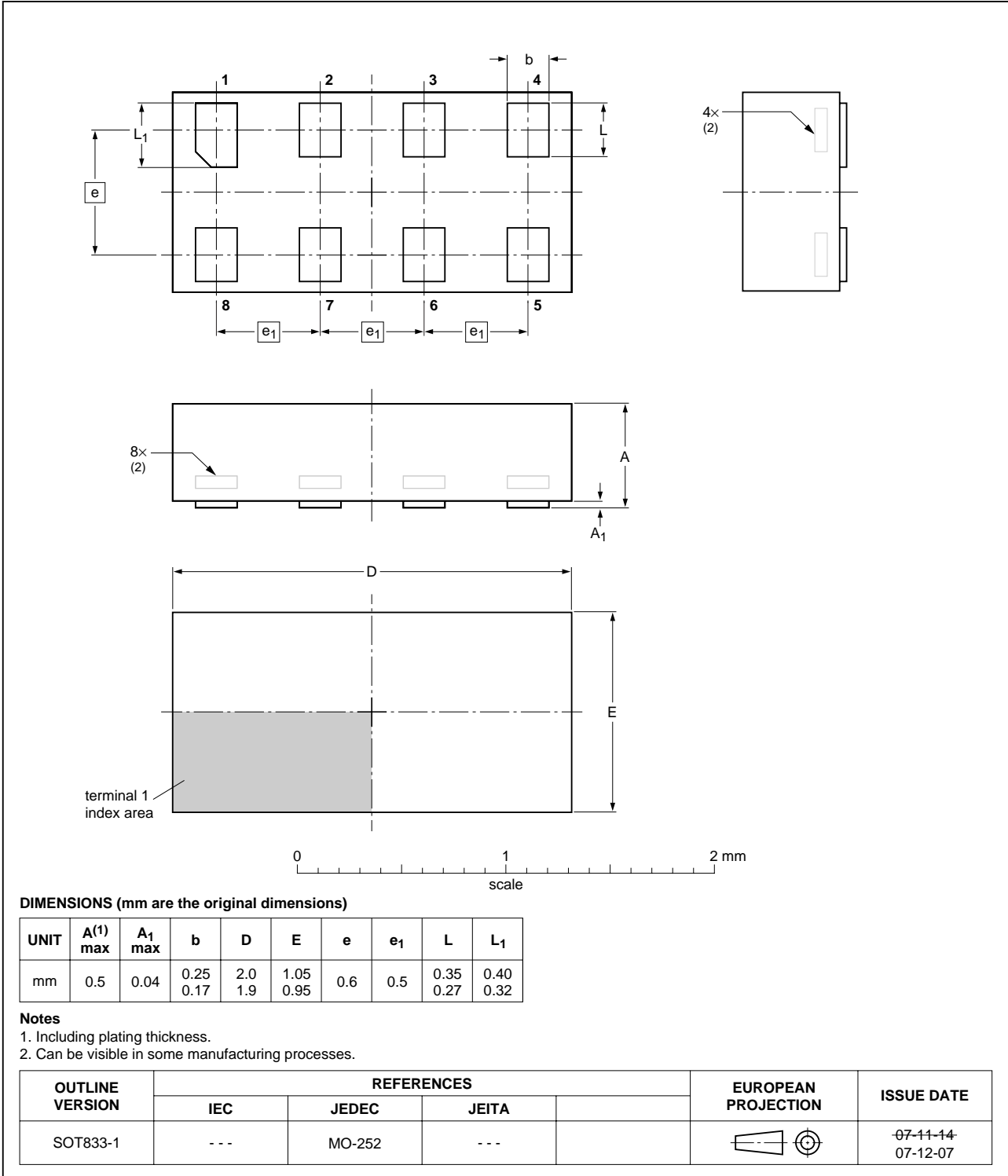


Fig 11. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads;  
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1



Fig 12. Package outline SOT902-1 (XQFN8U)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G240_4	20080229	Product data sheet	-	74LVC2G240_3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Figure 1</a> and <a href="#">Figure 2</a>: pin numbers removed from logic symbols</li> <li>• <a href="#">Figure 12</a>: package outline drawing updated to latest version</li> </ul>			
74LVC2G240_3	20071005	Product data sheet	-	74LVC2G240_2
74LVC2G240_2	20060728	Product data sheet	-	74LVC2G240_1
74LVC2G240_1	20030311	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 16.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

**18. Contents**

1 **General description** ..... 1

2 **Features** ..... 1

3 **Ordering information** ..... 2

4 **Marking** ..... 2

5 **Functional diagram** ..... 2

6 **Pinning information** ..... 3

6.1 Pinning ..... 3

6.2 Pin description ..... 3

7 **Functional description** ..... 4

8 **Limiting values** ..... 4

9 **Recommended operating conditions** ..... 5

10 **Static characteristics** ..... 5

11 **Dynamic characteristics** ..... 7

12 **Waveforms** ..... 8

13 **Package outline** ..... 10

14 **Abbreviations** ..... 14

15 **Revision history** ..... 14

16 **Legal information** ..... 15

16.1 Data sheet status ..... 15

16.2 Definitions ..... 15

16.3 Disclaimers ..... 15

16.4 Trademarks ..... 15

17 **Contact information** ..... 15

18 **Contents** ..... 16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 29 February 2008

Document identifier: 74LVC2G240\_4